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EXAMINER	
PARK, ILWOO	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	10/619,960	BIRAN ET AL.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 13-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11 and 13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/23/2007 have been fully considered but they are not persuasive. In the Remarks, Applicant argues as follows:

1.1 The present invention relates to controlling flow of data, via a memory, between first and second data processing systems such as a host computer system and a data communications interface for communicating data between the host computer system and a data communications network. [Specification: page 1, lines 8-11]

Thus, it is the intent that the meaning of a host system is a system that has one or more hosts. This differentiates a system from a singular host which is referred to in the specification as 'a host' or 'the host'.

For this point, the Examiner believes that a first data processing system shows a host computer system and a second data processing system shows a data communications interface which is quite different from the claim limitation, "said second data processing comprising a plurality of attached devices."

1.2 A conventional data processing network comprises a plurality of host computer systems and a plurality of attached devices all interconnected by an intervening network architecture such as an Ethernet architecture. The network architecture typically comprises one or more data communications switches. The host computer systems and the attached devices each form a node in the data processing network. Each host computer system typically comprises a plurality of central processing units and data storage memory device interconnected by a bus architecture such as a PCI bus architecture. [Specification: page 1, line 13-page 2, line 4]

Also, it shows that the specification does disclose that 'said second data processing system accessing the descriptor table comprises a plurality of attached devices.'

For this point, the Examiner disagrees. The Specification is not disclosing that a second data processing system comprising a plurality of attached devices accesses a descriptor table.

1.3 Thus, one aspect of the present invention, is to provide methods, apparatus and systems for controlling flow of data between first and second data processing systems via a memory. An example embodiment the apparatus comprising: a descriptor table for storing a plurality of descriptors for access by the first and second data processing systems; and, descriptor logic for generating the descriptors for storage in the descriptor table. The descriptors including a branch descriptor comprising a link to another descriptor in the table. The descriptor logic and descriptor table improve efficiency of data flow control between first and second data processing systems such as a host computer system and a data communications interface for communicating data between the host computer system and a data communications network. [Specification: page 2, lines 10-19]

Specification also does indeed disclose that 'said second data processing system which accesses 'the descriptor table' is shown to include embodiments wherein it comprises a plurality of attached devices.'

For this point, the Examiner disagrees. The Specification does disclose that said second data processing system accesses the descriptor table. However, the Specification does not disclose said second data processing system accessing the descriptor table comprises a plurality of attached devices. Rather, the Specification discloses that said second data processing system is a data communication interface for communicating data towards the network.

1.4 Viewing the present invention from another aspect, there is now provided a method for controlling flow of data between first and second data processing systems via a memory, the method comprising: storing in a descriptor table a plurality of descriptors for access by the first and second data processing systems; and, by descriptor logic, generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table. [Specification: page 3, lines 6-11]

Thus, the invention includes a plurality of descriptors for access by the first and second data processing systems, and a plurality of descriptor tables. These may represent tables from plurality of host computer systems.

For this point, the Examiner disagrees. The Specification does not disclose a plurality of descriptor tables. A single descriptor table is accessed by the first and second data processing systems.

1.5 In an embodiment, the apparatus includes: a descriptor table for storing a plurality of descriptors for access by the first and second data processing systems; and descriptor logic for generating the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link to another descriptor in the table. [Specification: page 5, lines 2-6]

A plurality of descriptors are stored in each of the plurality of descriptor tables.'

For this point, the Examiner disagrees. Again, the Specification does not disclose a plurality of descriptor tables. A single descriptor table is accessed by the first and second data processing systems.

1.6 Referring first to Figure 1, an example of a data processing network embodying the present invention comprises a plurality of host computer systems 10 and a plurality of attached devices 20 interconnected by an intervening network architecture 30 such as an InfiniBand network architecture (InfiniBand is a trade mark of the lnfiniBand Trade Association). The network architecture 30 typically comprises a plurality of data communications switches 40. The host computer systems 10 and the attached devices 20 each form a node in the data processing network. Each host computer system 10 comprises a plurality of central processing units (CPUs) 50, and a memory 60 interconnected by a bus architecture 70 such as a PCI bus architecture. [Specification: page 6, lines 4-12]

Thus, these devices indeed make up the a second data processing system which accessed the descriptor table in accordance with the specification description.

For this point, the Examiner disagrees. Again, the Specification does not disclose a second data processing system comprises a plurality of attached devices.

1.7 *Thus, it is apparent the specification of the present invention indeed by intent and in words teaches and discloses that 'said first data processing system (accessing 'the descriptor table') comprises a plurality of host computer system. Embodiments are included wherein 'said descriptor table' is accessible by either a single host computer system or by a plurality of host systems So it is apparent that the specification also does indeed disclose that 'said second data processing system (accessing 'the descriptor table') comprises a plurality of attached devices.'*

Thus, nowhere in the Specification discloses that a plurality of host systems accesses a descriptor table. The Specification does not disclose that the descriptor table stored in the memory in the apparatus is accessed by one host system accesses the descriptor table stored in the memory in the apparatus and another host system accesses the same descriptor table stored in the memory in the same apparatus. Nowhere in the Specification discloses that a second data processing system accessing a descriptor table comprises a plurality of attached devices. The Specification never discloses the plurality of devices 20 is included in a second data processing system accessing the descriptor table stored in the memory in the apparatus.

For this reason, the Examiner respectfully maintains the rejections.

2. Claims 1, 4, 5, 11, and 13 are amended and claims 2, 3, and 12 are canceled in response to the last office action. Osborne et al and Benner were cited in the last office action. Claims 1, 4-11, and 13-21 are presented for examination.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 4-11, and 13-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specification describes 'the first

data processing system' of claim as a host system including CPUs and a memory and 'the second data processing system' of claim as a data communication interface such as a network adapter 80 [page 5, lines 6-10; page 6, lines 10-12]; a 'descriptor table' is accessed by the first and second data processing systems. Specification further describes that there are a plurality of host computer systems and a plurality of attached devices [page 6, lines 4-8]. However, Specification does not disclose that the second data processing system (accessing the descriptor table) comprises a plurality of attached devices.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10, 14-16, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osborne et al. [US 5,751,951] in view of Benner [US 5,961,659].

As for claim 10, Osborne et al teach a method comprising controlling flow of data between first and second data processing systems via a memory, the steps of controlling comprising: storing [e.g., figs. 2A-2C and relevant description] in a descriptor table a plurality of descriptors for access [col. 3, lines 28-42] by the first and second data processing systems,

forming said first processing system to comprise a plurality of host computer systems ["computers" in col. 1, lines 20-25], said second data processing to comprise a

plurality of attached devices ["other networked computers and data systems" in col. 1, lines 20-25interconnected by an intervening network architecture, said network architecture comprises a plurality of data communications switches ["network switches" in col. 1, lines 13-20], said host computer system and attached devices each forming a node ["node" in col. 1, lines 13-20] in a data processing network, each host computer system comprises a memory interconnected by a PCI bus architecture ["PCI bus 152" in fig. 3A],

including a network adapter ["network interface card" in fig. 3A and relevant description] also connected to the bus architecture for communicating data between the host computer system and other nodes in the data processing network via the network architecture [col. 1, lines 13-30]; and

by descriptor logic, generating [e.g., col. 19, lines 46-47] the descriptors for storage in the descriptor table, the descriptors including a branch descriptor comprising a link [e.g., fig. 2A and relevant description] to another descriptor in the table.

However, Osborne et al do not expressly disclose that the host computer system comprises a plurality of central processing units. Benner teaches an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table [fig. 3B] wherein the first processing systems comprises a plurality of host computer systems [nodes 104 in fig. 1], each host computer system comprises a plurality of central processing units [microprocessors 106 in fig. 1] and a memory [main memory 108], and the second processing systems comprises a plurality of attached devices interconnected by an intervening network architecture [fig. 1]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to combine the teachings of Osborne et al and Benner because they both teach an apparatus for controlling flow of data between first and second processing systems via a memory having a descriptor table and Benner's teaching of multiple central processing units included in each host computer system of the first processing system would increase efficiency in processing [Benner: col. 4, lines 5-9] of the host computer of Osborne et al.

7. As for claim 14, Osborne et al teach the descriptor table comprising a plurality of descriptors lists sequentially linked together via branch descriptors therein [e.g., figs. 2A-2C and relevant description], wherein a branch descriptor comprises description of the descriptor location being link lists of descriptors, using information in the descriptors for control by software in the host of data movement operations performed by TX and RX LCP engines [TX 155, RX 157 in fig. 3A], using the information to process a frame to generate a TX packet header in the header of the frame ['frame descriptor" in col. 5, lines 53-65].

8. As for claim 15, Osborne et al teach the first data processing system comprising a host computer system [host in fig. 3A and relevant description].

9. As for claim 16, Osborne et al teach the second data processing system comprising a data communications interface for communicating data between a host computer system and a data communications network [host and network interface card in fig. 3A and relevant description].

10. As for claims 19 and 20, the combination of Osborne et al and Benner teaches the claimed limitations as discussed above.

Allowable Subject Matter

11. Claims 1, 4-9, 11, 13, 17, 18, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and amended to overcome the rejections under 35 U.S.C. 112, first paragraph, set forth in this office action.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park

January 31, 2008